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| EXAMINER |
|---|
| KENDALL, CHUCK O |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2192 | |

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/432,618 | ROEBER ET AL. | |
| | Examiner | Art Unit | |
| | Chuck Kendall | 2192 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15 and 28-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15, & 28-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This action is in response to the application filed 12/27/04.

2. Claims 1 – 15 & 28 – 44 are pending.

## Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 - 5, 12 - 15, 32 - 35 & 38 - 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rees et al. USPN 5,748,878 in view of Forum et al. USPN 6,519,638 B1.

Regarding claims 1 & 28, Rees discloses a system (Col. 16: 45 - 18: 20), and method (Col. 18: 20 - 22: 47), for monitoring the operation of computer program, by collecting related events relating to the performance of a plurality of target programs (7: 18 - 20, see probe tip 12), each program running on a respective target processor, and each target processor being located on a separate system bus, the system comprising: from a respective one of the plurality of target programs (4:1 - 10, and 6: 43 - 56 also see Col. 19: 45 - 50), wherein each of the plurality of event collection cards and the target processor running the respective one of the target programs is installed on the same system bus, and wherein each event collection card includes:

a time stamp clock for providing a time stamp when each event is received (fig3, 4.8);

an event memory for storing the received events (fig3, 4.6 and 4.4);

a sync interface unit for receiving a sync signal (fig 7, 180);

a collection control unit for time stamping the collected events according to the time stamp clock synchronized to the sync signal ***(12: 10 - 30, "A clock and control circuit 180 interfaces with the time stamp generator 102 (FIG. 3), a clock signal received from the probe tip 12 and control bits from the data reduction processor 114 ... Finally, a synch latch 198 latches in the time stamp at the appropriate time under control of the clock and control circuit 180 so that the time stamp is synchronized to the currently captured tag.')***, and for storing the time stamped events in the event memory, and for sending the collected software related events to a host computer the monitors the performance of the target program based on the collected events (3: 20 - 40, 5: 55 - 65,11:35 - 55, as well as FIG. 7. 180 and associated text Col. 12: 10 - 20). Rees doesn't explicitly disclose a plurality of event collection cards (probe tip from art), but Rees does mention in 7: 10 - 13, that "... the probe tip is usually specific to the particular microprocessor...". However, Forman in an analogous art discloses a plurality of collector probes (event collection cards) for collection events, see FIG. 2 and also synchronizing collected data, stating it is particularly important when an analyzer is examining different pieces of collected data corresponding to a particular time to determine what happened to a system at that time.

Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to combine Rees and Forman because, using a plurality of probes or collection cards would enable the system to monitor a plurality of target systems or programs.

Regarding claims 2 & 29, the system of claim 1, wherein the sync interface unit periodically receives the sync signal, and wherein the sync control unit periodically synchronizes the time stamp clock by setting the time stamp clock to a preset value upon receipt of the sync signal (Rees, fig7).

Regarding claims 3 & 30, the system of claim 2, wherein the sync control unit increments the time stamp clock to the preset value when the time stamp clock has not reached the preset value when the sync signal is received (Rees, 12:25 - 40).

Regarding claims 4 & 31, the system of claim 2, wherein the sync control unit stops the time stamp clock when the time stamp clock reaches the preset value before

the-sync signal is received (Rees, 12:25 - 40 for stop see latches at appropriate time, the latch is analogous to open and closing).

Regarding claim 5, wherein one of the plurality of event collection cards acts as a master card and at least one other event collection card including a slave card that synchronizes the time stamp clock of the slave card to the time stamp clock of the master card (Rees, 12:35-40, for master and slave see sync and under control of control circuit).

Regarding claim 12, the system of claim 1, wherein:

the collection control unit initializes the corresponding target processor prior to collecting events by assigning an address range to the target processor, wherein the target processor uses the assigned addresses when sending events to the event collection card (Rees, 6:40-45).

Regarding claim 13, the system of claim 12, wherein:

the collection control unit determines an identification value by decoding the address to which the respective target processor has sent the event, wherein the identification value corresponds to the target program corresponding to the respective target processor (Rees, fig 4, 132).

Regarding claim 14, the system of claim 13, wherein:

the collection control unit time stamps the identification value and stores the time stamped identification value in the event: memory (Rees, fig. 3, 4.6 and 4.4).

Regarding claim 15, the system of claim 1, wherein the collection control unit updates a memory count for each time stamped event stored in the event memory, wherein the event collection card sends the collected events to a host computer for processing, wherein the event collection card further includes (Rees, fig.3, 4.6 and 4.4, & 4.8):

a processing unit for sending the collected events to, the host computer according to the memory count (Rees, fig,7).

Regarding claim 32, see claim 5 for reasoning.

Regarding claim 33, see claim 6 for reasoning.

Regarding claim 34, see claim 8 for reasoning.

Regarding claim 35, see claim 9 for reasoning.

Regarding claim 38, see claim 12 for reasoning.

Regarding claim 39, see claim 13 for reasoning.

Regarding claim 40, see claim 5 for reasoning.

Regarding claims 41 & 43, Rees discloses all the claimed limitations as applied in claim 1 above. Rees doesn't explicitly disclose wherein the time stamp clock of each of the plurality of event collection cards are synchronized together, although Rees does disclose synchronizing the probe tips and stamp clocks for captured tags (events) 12: 25 - 30. Forman in an analogous art discloses a plurality of collector probes (event collection cards) for collection events, see FIG. 2 and also synchronizing collected data and allowing the collected data from the various probes to be synchronized together, stating it is particularly important when an analyzer is examining different pieces of collected) data corresponding to a particular time to determine what happened to a system at that time. Therefore, it would have been obvious to one of ordinary skills in the art at the time the invention was made to combine Rees and Forman because, using a plurality of probes or collection cards would enable the system to monitor a plurality of target systems or programs.

Regarding claim 42, the system of claim 1, Forman further discloses comprising: a clock source for sending the sync signal to each of the plurality of even collection cards (Forman, Co1.6: 35 - 42).

Regarding claim 44, the method version of claim 42, see rationale as previously discussed above.

5. Claims 6 - 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rees et al. USPN 5,748,878 in view of Forum et al. USPN 6,519,638 B1 as applied in claim 1 and claim 28 and further in view of Nouri et al USPN 6,073,255.

Regarding claim 6, Rees discloses, all the claimed limitations as applied in claim 1 and claim 28. Rees doesn't explicitly disclose a control unit receives a start request requesting that the collection control unit begin collecting events. However, Forman in a similar configuration and analogous art does disclose, " If the, probe indicates that it is

time to collect, a collect request will be enqued to the probe. Those probes whose time it is to collect can then start and collect in a synchronized matter." Forman, 8:60 - 67.

One of ordinary skill in the art would have made this combination because, synchronizing a plurality of event collection cards would enable the target systems to be monitored more time efficiently. The combination of Rees and Forman doesn't explicitly disclose whether the event collection card is a master card or a slave card. However, Nouri does disclose this limitation [Nouri, 11:23 - 30, 13: 25]. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Rees and Nouri, because sending requests or signals during synchronization makes syncing systems together more efficient.

Regarding claim 7, as in claim 1, wherein the plurality of event collection cards are daisy-chain connected to one another [Nouri, 11:35 - 40, see point to point serial link, see fig.2].

Regarding claim 8, the system of claim 1, wherein the sync interface unit receives the sync signal from a time-based global positioning system [Nouri, 10: 64 – 11:1 – 15, see Global network address].

Regarding claims 9, the system of claim 1, wherein the sync interface unit receives the sync signal from an atomic clock [Nouri, 10:64 –11:1 –15, see Global network address, interprets atomic clock to be the clock signal].

6. Claims 10, 11, 36 & 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rees et al. USPN 5,748,878 in view of Forman et al. USPN 6,519,638 B1 as applied in claim 1, and claim 28 and further in view of Hershey et al. USPN 5,375,070 hereinafter Hershey.

Regarding claims 10 & 36, Rees as modified by Forman discloses all the claimed limitation as applied in claim 1 and claim 28. The combination of Rees and Forman doesn't explicitly disclose a bus isolation unit for allowing the event collection bus and the local bus to operate in parallel. However, Hershey does disclose this feature in a similar configuration [Hershey, 12:30]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Rees with

Hershey to implement the instant claimed invention because, both deal with event logging (analogous, prior art) and provide similar solutions to the same problem.

Regarding claim 11, wherein the bus isolation unit allows the processing unit to access the event memory via the local bus and the event collection bus, see (Rees, fig 3).

Regarding claim 37, see reasoning in 11.

***Response to Arguments***

7. Applicant's arguments filed 12/27/2004 have been fully considered but they are not persuasive. Applicant argues on page 8 of Applicant's response that Rees and Forman cannot be combined to form a prima facie case of obviousness. Applicant further states that Forman is intended to monitor software and whereas Rees utilizes a hardware probe.

In responding Examiner does agree that Rees does utilize probes in the analysis process, however Rees does also utilize in its construction software based elements to analyze the target programs and hence the system contrary to Applicant's argument is in fact interchangeable. This can be seen in Rees in column 5: 20 – 45, where Rees teaches using instructions (software) during analyzing, see 5:20 – 30, "...Source code 60 written to run a target system is first instrumented by insetting tag statements 62 in the source code 10 at various locations that the user is interested in analyzing....in each branch of the source code 60, and the system 10 will determine which of the branches have been executed based on the whether each tag has been executed ". Examiner believes Rees does in fact show software based analyzing. And also contrary to Applicant's argument as pointed out in Applicant's response on page 8 last paragraph, regarding recited portions of Rees, Examiner believes that the cited paragraph as

indicated by Applicant regarding Rees, does not teach away from software based analyzing. The cited paragraph in Rees, 2: 10 – 12, merely recites the shortcomings of storing tag statement executions in system memory and does not have any substantial factual statements recited, that teaches away from software based analyzing. In fact Rees further discloses immediately after said statement in, 2: 15 – 20, that. *"...an ideal software analysis technique would be "transparent" to the target system and thus have no effect on the manner in which the target system executes software".* Furthermore, even if Applicant's notion is granted, there is no teaching or disclosure in Applicant's claims which exclude the use of hardware based analyzers.

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuck Kendall whose telephone number is 571-272-3698. The examiner can normally be reached on 10:00 am - 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WEI Y. ZHEN
PRIMARY EXAMINER